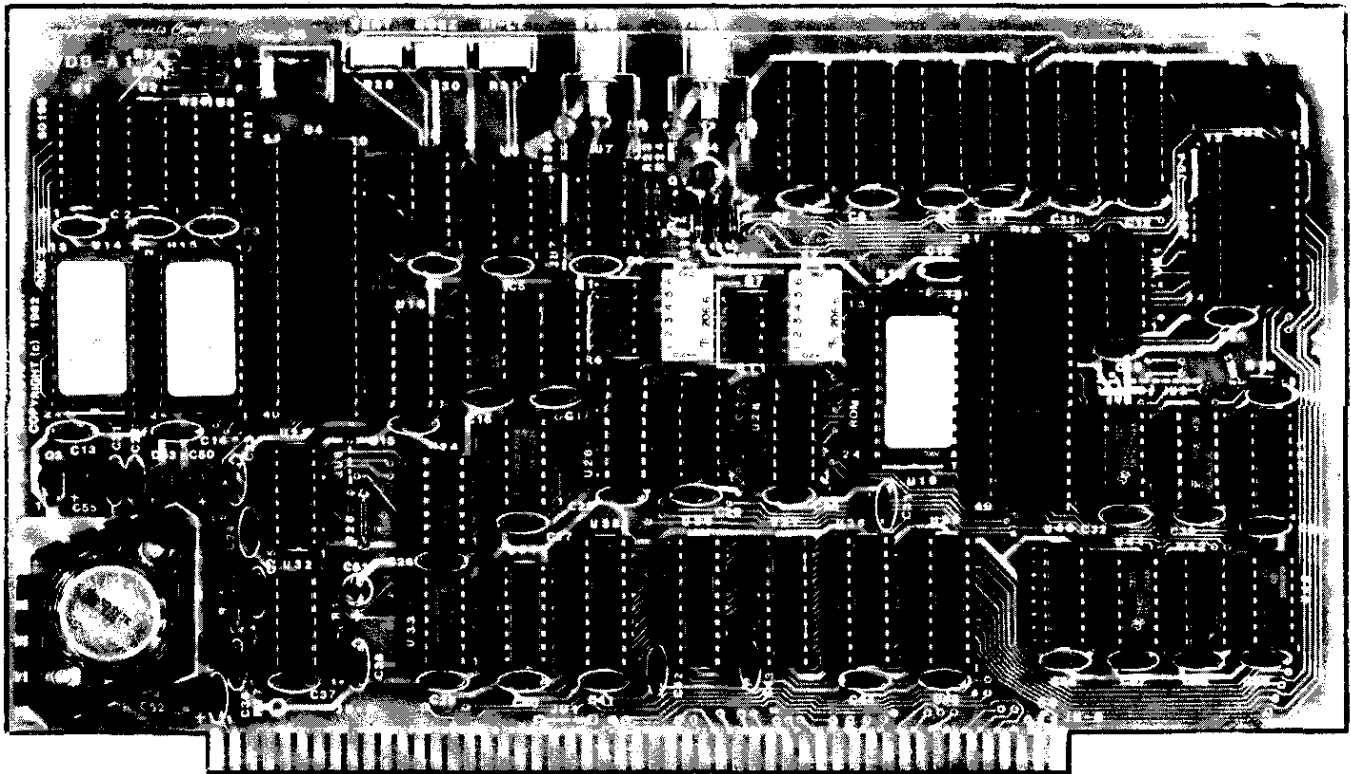


Simpliway Products Company

P.O. BOX 601
HOFFMAN ESTATES, IL 60195

V D B - A

S-100 VIDEO TERMINAL BOARD



The VDB-A is a video terminal interface for S-100 based computer systems. It provides a totally programmable C.R.T. display, including: an 80 character by 24 line display, blinking cursor, highlighted/blinking text formatting, etc. The Intel 8275 C.R.T. Controller is fully implemented, including the light pen feature (via software linkages in the program eprom). A complete parallel-input keyboard port is provided, and a portion of the on-board 2114 static ram is used to allow the user to type commands ahead to the host computer while it is executing other code. The on-board Z80 CPU and 2 kbyte program eprom provide lightning fast keyboard and video operations.

A second 2716 eprom provides the full ASCII character set with lower case descenders, while an optional third eprom may be used for an alternate character set or custom graphics. Pre-programmed eproms can be purchased separately. The on-board ram (3 kbytes) is used for the keyboard buffer, video and attribute data, and scratch pad/stack for the CPU.

The board may be configured as either I/O port, or memory mapped, and may be changed from one to the other under keyboard or software control. In the I/O mode, the on-board ram is not addressable by the host CPU (ie: does not occupy system memory map), and all video and screen attribute data flow through the I/O ports. In the memory mapped mode, the I/O port is still fully active; the screen portion of the ram may be written to by either the host CPU, or through the I/O port, although the video data ram may not be directly read by the host CPU.

Thus, the on-board ram occupies a portion of the system memory map, but only as "write-only" memory. It is required however, that the memory in the host system be tolerant of wait states, as some operations will be delayed by screen refresh periods. The VDB-A does not use direct memory access (DMA), and thus compatibly resides in most S-100 systems. This eliminates such things as bus conflicts during disk operations, etc. The design presumes a 2 MHz system clock, although 4 MHz is permitted with the use of faster rams and eproms, or the use of an on-board divide-by-two circuit.

The software provided features complete cursor control and addressing, up to 16 attribute changes per line (ie: blinking, reverse video, highlight, underline, etc.). The software emulates the Micro-Term (TM) ACT-4 terminal, but can be easily modified for others. While the IEEE-696 bus definitions are observed, the higher address pages are not decoded, and systems of more than 65 Kbytes could experience difficulties.

The PC board is of high quality, with plated thru holes, solder plated runners, solder masks on both sides, a component side legend, and gold plating on the edge connector.

OTHER FEATURES include:

- Bell (beeper) driver for direct connection to a speaker
- Separated video and sync, or composite video
- I/O port and screen addressing individually switch selectable
- Choice of positive or negative keyboard strobe
- Keyboard port socket (16 pin dip) also provides +5 v. and -12 v. to power keyboard
- All static ram ('2114's , 300 ns.)
- Documentation includes : 49 pages of schematics and parts list, theory of operation, construction hints, a well annotated source listing of the "ROM 1" video driver software, the bit pattern listing for the "ROM 2" character generator eprom, and trouble shooting chart.
- Easily configured to allow emulation of most terminals by modification of video driver software.
- NEW OPTIONAL 25 line non-scrolling for STATUS DISPLAY (Note: deletes underline attribute)
- Optional interrupts output, "AND MUCH MORE".

Please note:

The VDB-A is a somewhat complex product, and its construction should not be attempted by those without some previous experience in assembling and testing circuits of similar complexity. Should you feel un-sure, please order the documentation package first.

VDB – A VIDEO TERMINAL

FOR S-100 SYSTEMS

USER'S MANUAL

SIMPLIWAY PRODUCTS COMPANY

*P.O. Box 601
Hoffman Estates, Il. 60195
(912) 959-7997*

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Please note:

The VDB-A is a somewhat complex product, and its construction should not be attempted by those without some previous experience in assembling and testing circuits of similar complexity. Should you feel it is too difficult a project, please feel free to return the complete un-assembled product for a cash refund, after obtaining prior permission from SPC.

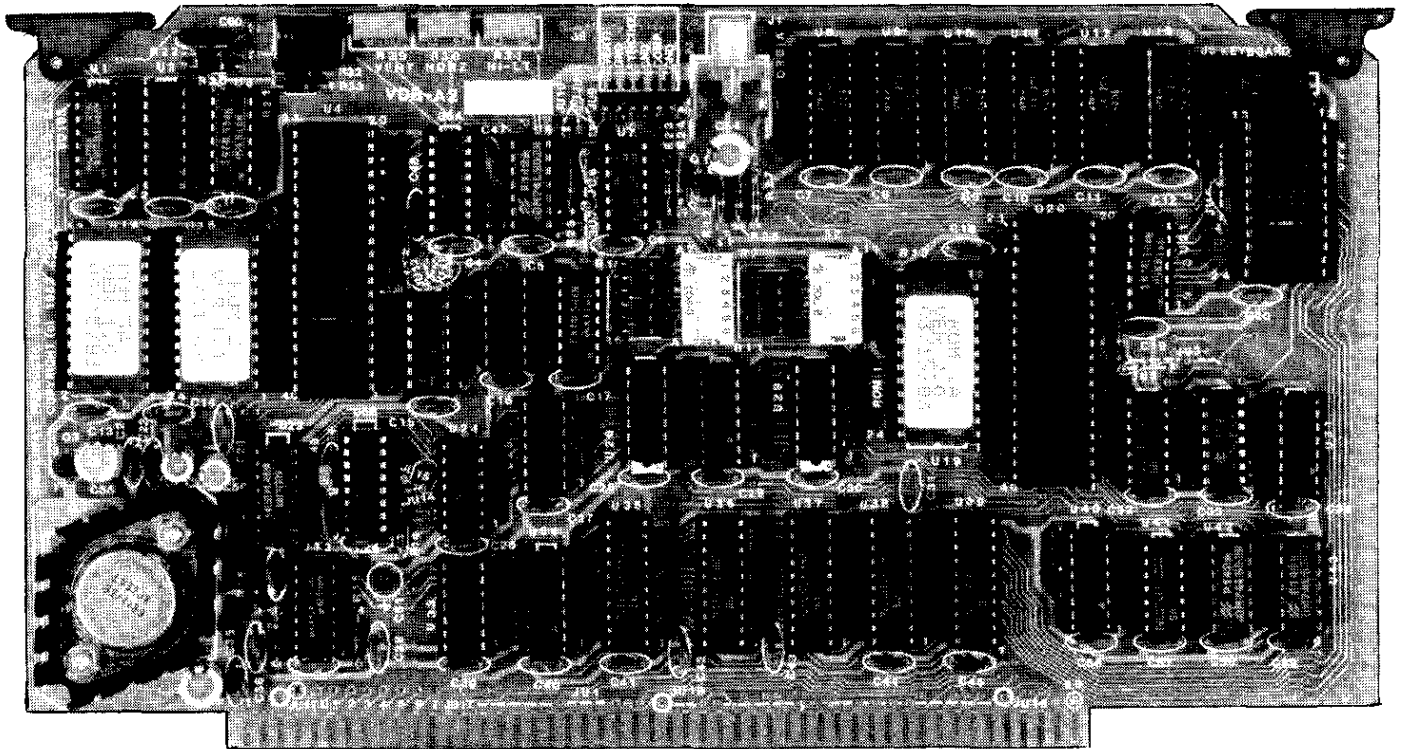
*** SPECIAL NOTE ---- Monitor Requirements ***

Like many other high performance video display boards, the VDB-A Video Board must be used with a monitor that has a high video bandwidth (at least 12 MHz), and is capable of operating at a 19 kHz horizontal sync rate. If the monitor to be used cannot be adjusted externally for this higher sync rate, then internal modifications (usually quite simple) will be necessary. Please refer to the note on page 12, and the Trouble-shooting chart for more information. Alternatively, the 25 line software option may be ordered.

INTRODUCTION and SPECIFICATIONS

V D B - A

S-100 VIDEO TERMINAL BOARD



THE MANY FEATURES of the VDB-A include:

- WORDSTAR & dBASE II compatability for highlighted display *
- 25th non-scrolling status line - TIME STAMP or SOFT KEYS *
Note: Deletes underline attribute; allows 15,750 kHz sync
- All 8275 attributes available: BLINK, HIGHLIGHT, REVERSE VIDEO, and UNDERLINE (rel's 1.x & 3.x only)
- Bell (beeper) driver for direct connection to a speaker
- TYPE-AHEAD keyboard buffer holds 80 characters
- Alternate character eeprom socket, software controlled
- Separated video and sync signals, or composite video
- Memory mapped screen addressing is switch selectable to any 2K boundry, and enabled under host system control
- I/O port addressing switch selectable to any group of 4
- Choice of positive or negative keyboard strobe
- Keyboard socket provides +5 and -12 v. to power keyboard
- All static ram ('2114's , 300 ns.)

WORDSTAR is a trademark of Micropro International Corp.

dBASE II is a trademark of Ashton-Tate Corp.

VDB-A and VIDSTAR are trademarks of The Simpliway Products Co.

- Easily reconfigured to allow emulation of most terminals by modification of video software: Televideo 920 is standard.
- Optional interrupts output, "AND MUCH MORE".

* Requires optional software --- See ordering info page

The VDB-A is a video terminal interface for S-100 based computer systems. It provides a totally programable C.R.T. display, including: an 80 character by 24 line display, blinking cursor, highlighted/blinking text formatting, etc. The Intel 8275 C.R.T. Controller is fully implemented, including the light pen feature (via software linkages in the program eeprom). A complete parallel input keyboard port is provided, and a portion of the on-board 2114 static ram is used to allow the user to type commands ahead to the host computer while it is executing other code. The on-board Z80 CPU and 2 kbyte program eeprom provide lightning fast keyboard and video operations (over 19,000 baud!).

A second 2716 eeprom provides the full ASCII character set with lower case descenders, while an optional third eeprom may be used for an alternate character set or custom graphics. Pre-programmed eeproms can be purchased separately. The on-board ram (3 kbytes) is used for the keyboard buffer, video and attribute data, and scratch-pad / stack for the CPU. The board may be configured as either an I/O port or memory mapped, and may be changed from one to the other under keyboard or software control. In the I/O mode, the on-board ram is not addressable by the host CPU (ie; does not occupy system memory map), and all video and screen attribute data flow through the I/O ports. In the memory mapped mode, the I/O port is still fully active; the screen portion of the ram may be written to by the host CPU directly or through the I/O port. Although direct reading of the video ram by the host CPU is not supported, it is possible to do.

Thus, the on-board ram occupies a portion of the system memory map, but only as "write-only" memory. It is required however, that the memory in the host system be tolerant of wait states, as some operations will be delayed by screen refresh periods. The VDB-A does not use direct memory access (DMA), and thus compatibly resides in most S-100 systems. This eliminates such things as bus conflicts during disk operations, etc. The design presumes a 2 MHz system clock, although 4 MHz is permitted with the use of faster rams and eeproms. The software provided features complete cursor control and addressing, and up to 16 non-displayed attribute changes per line (ie: reverse video, blinking, highlight, underline, etc.) in any combination. The software emulates the Micro-term (tm) ACT-4 (VDB-A software version 1.x) or the TELEVIDEO 910/920 (versions 3.x & 4.x) terminals, but can be easily modified for others. While the IEEE 696 bus definitions are observed, the higher address pages are not decoded, and systems of more than 65 Kbytes could experience difficulties, unless certain system software precautions are observed, and then only when in the memory-mapped mode.

The FR4 PC board is of high quality, with plated thru holes, solder plated runners, solder masks on both sides, a component side legend, and gold plating on the edge connector.

ASSEMBLY INSTRUCTIONS

Start by obtaining a small needle nose pliers and wire cutter, a screwdriver, a flat work surface, and a strong light. A rosen core solder is mandatory for printed circuit work, and the thinner .040 diameter type is preferred. Use a 25-40 watt soldering iron with a small chisel or pencil tip. Apply the iron to the circuit pad to be soldered, apply the solder to the pad, touching the iron as well, and add enough solder to wet the tip and pad. Hold the iron on long enough to cause the solder to bubble down into the plated thru hole. If not enough heat is used, flux may form around the component lead and leave an intermittent or cold solder joint. If too much heat is used, the foil pad will lift off the board, and the component may be damaged as well.

The general procedure is to start with those components that have the lowest profile (height), then add the next lowest parts, etc., until all the components are soldered. The component side of the board has the component legend. Insert the leads of the component into the correct holes as shown by the legend (and printed component placement guide), seat the part as close to the board as possible, and bend the leads over at about a 45 degree angle. Then solder as described above and clip the leads as close as possible to the board. The recommended order of assembly is as follows:

First, examine the board for visible shorts. If possible, use an ohmmeter to check for shorts between address lines, data lines, and between +5 v. and ground (pins 1 & 50) on the edge connector.

Insert all 1/4 watt resistors:

<input checked="" type="checkbox"/> R1-R14	10.0 kohm	(brown-black-orange)	<input checked="" type="checkbox"/> R20	220 ohm	(red-red-brown)
<input checked="" type="checkbox"/> R15	220 kohm	(red-red-yellow)	<input type="checkbox"/> R16	68 kohm	(blue-gray-orange)
<input checked="" type="checkbox"/> R17	6.8 kohm	(blue-gray-red)	<input checked="" type="checkbox"/> R18	4.7 kohm	(yellow-violet-red)
<input checked="" type="checkbox"/> R21	560 ohm	(green-blue-brown)	<input checked="" type="checkbox"/> R22	1.5 kohm	(brown-green-red)
<input checked="" type="checkbox"/> R23,24	470 ohm	(yellow-violet-brown)	<input checked="" type="checkbox"/> R25,19	330 ohm	(orange-orange-brown)
<input checked="" type="checkbox"/> R26	75 ohm	(violet-green-black)	<input checked="" type="checkbox"/> R27	150 ohm	(brown-green-brown)
<input checked="" type="checkbox"/> R28,32,33	2.2 kohm	(red-red-red)			

Turn the board over, lay it on a flat surface and solder all resistors.

Insert all IC sockets, noting the proper position of pin 1 on each (usually a notch in the plastic). Sockets should not be used for switches S1 and S2. Place a heavy cardboard (the back of a clip-board does nicely) over the sockets, and carefully turn the sandwich over to expose the solder tails of the sockets. Solder only adjacent pins of each socket (ie: pins 1 & 8 on a 14 pin socket). Now the board can be lifted without the sockets falling out. Re-heat each joint, forcing the socket down against the board to seat it properly. All this is to insure that the sockets won't tear foil loose when the IC's are inserted. After this, the rest of the pins on the sockets can be soldered.

Insert and solder the 79L12 regulator, Q3. Observe the marking on the board. Note: if -12 volts is not required on the keyboard socket, this part may be deleted.

Insert and solder all disk ceramic capacitors:

<input checked="" type="checkbox"/> C1-C45, C56-59	0.01 uF, 25 v.	<input checked="" type="checkbox"/> C46,49	.047 uF, 25 v.
<input checked="" type="checkbox"/> C47	.001 uF, 25 v.	<input type="checkbox"/> C48	470 pF, 25 v.
<input type="checkbox"/> C60	33 pF, silver-mica		

Insert and solder the tantalum and electrolytic capacitors, noting the polarity sign (+) marked on the board:

<input type="checkbox"/> C50,52-55	15 uF, 20 v.	<input type="checkbox"/> C51	1.0 uF, 20 v.
------------------------------------	--------------	------------------------------	---------------

Insert and solder the potentiometers:

<input type="checkbox"/> R29,30	20 kohm
<input type="checkbox"/> R31	5 kohm

Insert and solder Q1, the 2N3904 transistor, being sure to position the emitter (E), base, and collector (C) leads correctly.

- [] Mount the phono connector and solder. Also, assemble the coax cable to the plug (optional).
- [] Mount Q2, the LM323, 5 volt regulator and its heatsink. The two screws used for the flange also mount the heatsink as well. Do not use an insulator under the device, but a very thin coating of heat conducting grease (Wakefield) between the device flange and the heatsink is quite desirable. The heads of the screws should be located on the solder side of the board, and care should be taken to not over-tighten them. The leads of Q2 may now be soldered.
- [] Bend the leads of the crystal, taking care not to stress the points where the leads enter the bottom of the crystal case. Insert and solder. A small piece of double-sided foam tape makes an excellent retainer and shock mount.
- [] Insert and solder the jumper options as described below:
 - [] JU1 For non-maskable interrupts to host CPU
 - [] JU2 For 2 MHz system clock (standard S-100)
 - [] JU3 For 4 MHz clock (non-standard & seldom used)
 - [] JU4 If keyboard strobe is positive
 - [] JU5 If keyboard strobe is negative
 - [] JU6,9,13,15 For composite video output to connector J1
 - [] JU7,9,13,15 For video output to J1 and sync output to J2
 - [] JU7,10,12,15 Separated video, horiz, & vert to J2 ***
 - [] JU8 To NOT invert the signal from the light pen
 - [] JU16 To use "preset" instead of "PDC". Also cut the runner at pin 99 of the S100 edge connector.
 - [] JU17 To use Vectored Interrupts, VI 0 thru 7
- [] Insert and solder switches S1 and S2.
- [] Perform a thorough visual check of the board under a strong light to locate and clear any solder bridges between adjacent pads.
- [] Insert board into host system and apply power. Observe that +5 volts appears on each IC socket pin as described in the parts listing. Also check that +5 volts appears on pin 16 of the keyboard socket, and that there is -12 volts on pin 14, if Q3 is installed. Note that this pin can only source about 100 mA to the keyboard.
- [] Turn off the power, remove the board from the system, and with the board lying on a conductive, grounded surface, insert all IC's into their sockets, using the component placement guide and parts list. Take extreme care to insert each IC in the correct direction, and to observe that none of the leads of the IC's fold up under the body (a very common occurrence, and very hard to see!).

***** SPECIAL NOTES *****

The Z80 CPU, 8275 CRT controller, the 2114 rams, and the 2716 eeproms are STATIC SENSITIVE devices. Static preventive measures MUST be employed.

- [] By this time, you should have prepared (or purchased) the program ROM (1) and the character generator ROM (2). Insert these as well.
- [] Replace the board into the system, and connect the monitor RF coax to J1 (or J2 if using separate sync).
- [] Apply power, and using a thumb or forefinger, quickly check the body of each part for overheating. Only the regulator Q2 should get noticeably warm after a minute or so. If any other part gets very warm, the part may be defective or inserted wrong. Turn the power off immediately and correct this!

[] Adjust the 20 kohm pots (R29 and R30) to obtain a raster on the CRT. R30 controls the horizontal sync and position, and R29 controls the vertical sync. When adjusted properly, the cursor should be observed flashing in the upper left-hand corner of the screen.

[] Remove the power. If the on-board keyboard port is not to be used, skip the rest of this section.

Connect the keyboard to the socket, using a 16 pin dip plug and cable wired as follows:

Pins 1 thru 7 of this socket correspond to the ASCII parallel data bits 0 - 6 respectively. Wire these accordingly. Connect the keyboard strobe line to pin 9 of the socket, and use both pins 11 & 12 for the ground (common) return. Power for the keyboard is available on pin 16 (+5 v) and pin 14 (-12 v), when installed.

[] A speaker (8 ohms or greater) may be connected to pin 15 of the keyboard socket. A 1000 ohm volume control, mounted on the keyboard, and wired in series with the speaker, is often desirable.

[] Switch block S1 sets the I/O port address of the board. Position 1 represents the highest order bit (A7) of the address; position 2 - A6; etc. The software supplied assumes the board is addressed at ports F0 to F3 (although F3 is not used), and thus the switch would be set as follows:

A7	A6	A5	A4	A3	A2	
						ON = 0
1	2	3	4	5	6	
						OFF = 1
OFF	OFF	OFF	OFF	ON	ON	

If this port assignment conflicts with the host system assignments, the polling program (described below) and the port equates in the CRTLOOP listing (or host system driver patch) must be redefined. Also, the S1 switch block must be set accordingly.

[] Switch block S2 sets the memory mapped address of the screen ram (2 Kbytes) at any 2K boundary. Thus, if the screen is to be addressed at C000 to DFFF, the switch settings would be:

A15	A14	A13	A12	A11	
1	2	3	4	5	6
OFF	OFF	ON	ON	ON	X

X = Not Used

[] With the board properly address, and with all required IC's and jumpers installed, replace the board into the system (power off, of course), install the keyboard plug and the CRT cable plug(s) as described above.

[] Apply the power again, and with the cursor flashing, enter by some means a short program that will read the keyboard and display the keyboard data. Refer to the sample program furnished, CRTLOOP, for a basic example. In this program, both the on-board keyboard port and a system keyboard port are polled. In say, a CP/M system, a routine similar to this would be part of the CBIOS.

*Trademark of Digital Research Corp.

[] Execute the small program previously loaded into system ram, and observe the CRT's response to the keyboard as you press each key. The system should be acting as a video typewriter, with only the I/O ports active.

- [] Next, try the escape and control codes. The cursor should be moveable, and the flashing, underlining, etc., should be operable. Refer to the QUICK REFERENCE CHART for the definitions of each code, as defined by the ROM 1 software supplied. NOTE: Except for the memory map commands, all escape and control codes are toggle entries, ie: on & off, and effect only keyboard entries following each command.
- [] Adjust the contrast and brightness controls of your monitor device for the best overall character definition. Remember, a converted TV set will not provide the high resolution of a wide bandwidth video monitor unit. Again, only characters typed after invoking a control or escape code will be displayed in that fashion.
- [] With the highlight mode enabled (^N), type a string of characters. Adjust R31 for the desired brightness, relative to characters typed with the highlighting disabled. Alternate control-N's (^N) will enable, then disable, the highlighting function for succeeding keystrokes. NOTE: the ROM 1 software initializes the board to the 'bright' condition. (Note: Release 1.x software is presumed in this text)
- [] Now enter an esc-M from the keyboard. This enables the memory mapped mode. Until an esc-O is entered, the on-board ram occupies a part of the system memory map, at the address assigned by switch block S2.
- [] With the speaker connected as described previously, activating a control-G (^G) should produce a pleasant tone. A ^L (formfeed) will clear the screen.

The VDR-A should be working properly when all these checks have been successfully completed. A *troubleshooting chart* is included in this document to assist in locating some hardware faults. We recognize that it may be difficult to diagnose faults on a product of this type, since the program cannot be modified directly by the host system to assist in isolating problem areas.

If a problem occurs that seems to defy easy solution, PLEASE, PLEASE call or write us. If you find a solution to a problem, again, let us know about it, as we may be able to pass it along to others similarly troubled.

Theory of Operation for the Video Display Board

General Description

The Video Display Board (VDB-A) is a self contained computer terminal, less the monitor and keyboard. The display is comprised of 24 lines of 80 columns, and uses the Intel CRT Controller 8275 and a Z80 microprocessor to control the functions. The 8275 provides cursor control, reverse video, blinking, underlining, highlighting, and light pen function. The displayed characters are in a 5 X 7 format with upper and lower case. Two character generators are available to the user. The board may be interfaced to the host computer via an I/O port or memory mapped mode. The keyboard interface is 8 bit parallel with strobe and a 80 character type ahead buffer. A speaker oscillator circuit is also provided for the audible "bell" tone.

The VDB-A may be divided into five logic blocks: S-100 interface, Microprocessor and control logic, system memory, video display circuits, and memory map circuit. Each block will be discussed below.

S-100 Interface

This portion of the VDB-A provides the I/O interface to the S-100 bus. The Interface uses three I/O addresses whose upper six bits are determined by the dip switch block (S1) connected to the decoder U-26. The two remaining least significant bits perform the following functions:

- 00 Display port status (IN), Display data (OUT)
- 01 Keyboard status (IN).
- 10 Keyboard data (IN).

For example, if the dip switches were set to 00H then the address 80H would read the keyboard status.

The VDB is selected by a correct address presented to U-26 which in turn enables U-34. U-34 is also enabled by SIN or SOUT via a NOR gate. When a display port status is desired pin 15 of U-34 is low and DRIN is high. This allows the port status stored in flip-flop U-24 to be put on the S-100 bus via the tri state gate U-17. The keyboard status is read in the same manner. When the host computer writes to the display, pin 14 of U-34 is low and PWR* is low. This activates the latch U-38 to accept the data on the S-100 bus and hold it for the Z80, and it also sets the status flip-flop U-24. When the host computer reads the keyboard, pin 13 of U-34 is low and DBIN is high. This puts the data stored in latch U-39 on the S-100 bus, and resets the status flip-flop U-24.

The Z80 also writes to U-39, and reads U-38 and the status latches. This is done through the I/O decoder, U-40 and U-33.

Microprocessor and control logic

The Z80 processor controls all of the functions of the VDB-A via the internal address and data buses. Eight I/O ports are addressed via decoder U-40. These functions are:

- S-100 interface status (2 ports)
- S-100 display data (IN)
- S-100 keyboard data (OUT)
- Keyboard latch
- Speaker oscillator circuit
- Memory map ports
- 8275 CRT Controller
- Interrupt flip-flop

There is also special interface circuits to transfer display characters to the 8275. When the 8275 wants data for the next line to be displayed, pin 5 of the 8275 goes high. This sets the flip-flop U-29, which generates an interrupt in the Z80. The Z80 transfers the data to the 8275 by reading the refresh memory. The Z80 tells the 8275 to latch the data by activating pin 5 on the Z80 (A15). This pin is fed to U-43, along with the read signal and the data request from the 8275. The output of U-43 goes low telling the 8275 to latch the data via pin 6 and pin 10, data acknowledge and WR*. When the transfer is finished, the interrupt flip-flop is reset by the Z80.

The keyboard latch is activated by the strobe produced by a parallel keyboard. Once the data is latched, an interrupt is sent to the Z80 processor, which in turn reads the latch.

When the speaker oscillator U-32 is activated by decoder U-40, a 1kHz tone is produced for 500ms.

System Memory

The system memory consists of 2k of ROM and 3k of RAM. The ROM 1 contain the VDB-A control program. The RAM is used for the display refresh memory, keyboard buffer, and control program scatch pad area. All of memory is addressed via the decoder U-31 and the Z80 control lines WR* and MREQ*.

Video Display Circuits

The video display circuits are controlled by the 8275 and the dot clock oscillator. The oscillator is made up of inverters in U-3 and a 13.63 MHz crystal. This output is called the dot clock, and is used to drive the parallel-to-serial shift register, U-1, and the divide by seven, U-2. The output of U-2 is called the character clock, since its period is the width of one character on the screen. The character clock drives the logic in the 8275 to produce the video timing signals. At the rising edge of the character clock, the next character to be displayed is presented to the character generator. On the falling edge of the character clock, the output of the character generator is latched into the shift register, U-1, where the data is serially shifted by the dot clock to the monitor. Before the character is presented to the monitor it is combined with other timing signals from the 8275. These are latched into U-23 on the falling edge of the character clock. These signals are:

- Reverse video
- Video suppression (used during horizontal and vertical retrace, and blinking)
- Light enable (used to display the cursor and underline)
- Highlight
- Horizontal Retrace
- Vertical Retrace

The Horizontal and Vertical retrace pulse widths are controlled by U-5A & B to match most monitors. Also, these signals can be separated from the video data.

Memory Map Interface

The memory map interface used with VDB-A does not access the display memory directly from the S-100 bus as in most systems. This is because the memory is not organized in the same manner as most memory mapped video boards. When the host computer wishes to put a chracter on the screen, the address and data are latched. The latched data is then read by the Z80 processor, which then calculates then proper display address and puts the character on the screen. If the host computer tries to output another character before the Z80 processor has read all of the latches, the S-100 ready line is forced low until the last latch is read.

Address decoding is by the comparator, U-28. The switch block (S2) connected to U-28 allows the user to set the memory map in 2 kbyte increments. The decoder is only activated by a memory write cycle. When a proper address is decoded by U-28, U's 36, 35, and 37 are latched. The address and data is latched by PWR*, and the latch status flip-flop U-41 is set. This tells the Z80 processor that there is a new character to be placed, causing it to read the latches, through the decoder, U-27. Also, when latch U-37 is read, the status flip-flop is reset. If the status flip-flop is set and the host computer wishes to place a character, the ready line is set low via the address decoder and U's 42 and 7.

*** SPECIAL NOTE on monitor requirements ***

In order to get 12 scan lines per character row (needed for lower case descenders and underlining), a horizontal sync rate of 18.720 kHz is used, which is much above the 15.750 kHz normally associated with TV systems. The monitor selected to be used with the VDB-A Video Board must be capable of operation at this higher sync rate, and may require an internal modification to the horizontal oscillator (usually quite simple), if the external adjustment on the monitor does not have enough control range. If the sync frequency is incorrect, multiple cursors, spread out characters, etc. will be displayed.

IC#	DESCRIPTION	STRAPPED PINS	
		5V	GND
30	74LS00	14	7
42	74LS02	14	7
6	74LS02	14	7
25	74LS32	14	7
33	74LS32	14	7
18	74LS04	14	7
21	74LS04	14	7
3	74LS04	14	7
7	74LS05	14	7
16	74LS86	14	7
24	74LS74	14	7,2,3,11,12
29	74LS74	14,4	7
41	74LS74	14,10,4	7
26	8131	16	7,8
28	8131	16	8,1,2
34	74LS138	16,6	8,3
40	74LS138	16,6	8,5
31	74LS138	16,6	8,5
27	74LS138	16,6	8
39	74LS373	20	10
37	74LS373	20	10
35	74LS373	20	10
38	74LS373	20	10
36	74LS373	20	10,8,13,14,17,18
17	74LS125	14	7
32	556	14	7
22	8212	24	12,2
20	Z80	11,24,25	29
4	8275	40	20
8	2114	18	9
9	2114	18	9
10	2114	18	9
11	2114	18	9
12	2114	18	9
13	2114	18	9
19	2716 *	21,24	12,18
15	2716 *	21,24	12,18
14	2716 *(OPTIONAL)	21,24	12,18
1	74LS166	16	8
23	74LS174	16,1	8
2	74LS161	16,1,3,6,7,10	8,4,5
5A	74LS123	16,3,11	8,1,9
5B	74LS123	16,3,11	8,1,9
43	74LS20	14	7

* AVAILABLE PRE-PROGRAMMED FROM THE SIMPLIWAY CO.
 NOTE: Use single supply, 5 volt type only.

MISC. COMPONENTS

QTY	DESCRIPTION
1	LM323 5v, 3a TO3 CASE
1	* HEAT SINK THERMALLOY #6013-B
2	40 PIN SOCKET
5	20 PIN SOCKET
4	24 PIN SOCKET
6	18 PIN SOCKET
12	16 PIN SOCKET
16	14 PIN SOCKET
1	3 FT 16 PIN DIP CABLE (FOR KEYBOARD)
49	.01uF CAPS, DISK 25V +80/-20%
5	15uF TANT CAPS 20V +/- 20%
1	1.0uF TANT CAP 20V +/- 10%
1	.001 uF CAP, DISK 25V +/- 10%
2	.047 uF CAP, DISK 25V +/- 10%
1	470 pF CAP, DISK 25V +/- 10%
1	33.0 pF CAP, Silver mica +/- 10% style DM15
1	68K OHMS 1/4W 5%
1	6.8K OHMS 1/4W 5%
1	220K OHMS 1/4W 5%
1	220 OHMS 1/4W 5%
1	150 OHMS 1/4W 5%
1	75 OHMS 1/4W 5%
1	560 OHMS 1/4W 5%
1	1.5K OHMS 1/4W 5%
2	470 OHMS 1/4W 5%
2	330 OHMS 1/4W 5%
14	10K OHMS 1/4W 5%
1	4.7K OHMS 1/4W 5%
3	2.2K OHMS 1/4W 5%
1	* 5000 OHM POT 3/8" SIDE ADJUST, STANDUP, 0.15" SPACING,
2	* 20K OHM POT (BOURNS SERIES 3386S OR EQUIV.)
1	* CRYSTAL: 13.628 MHz (60 Hz USA) ROM-1 ver.: 1x & 3x
	11.356 MHz (50 Hz FOREIGN) " "
	11.340 MHz (60 Hz USA) 2x & 4x
	9.450 MHz (50 Hz FOREIGN) " "
	Note: Frequency also determined by ROM-1 version used.
1	NPN TRANSISTOR 150 MHZ Ft 2N3904 OR EQUIV.
1	REGULATOR, -12.0 VOLTS, MC79L12 OR EQUIV.
2	6 POSITION DIP SWITCH
1	6 POSITION PIN HEADER Molex #22-05-3061, GC# 41-046 (Opt'l)
1	* P.C. PHONO JACK (OPTIONAL)
2 EA.	6-32 X 3/8" ROUND HEAD MACHINE SCREW, NUT, LOCKWASHER
2	Ejectors Scanbe, Inc. # S-203 or equiv. (Optional)
	* AVAILABLE FROM THE SIMPLIWAY CO.

SOFTWARE OVERVIEW

VIDEOxx.PRN ---

This is the complete source listing of the ROM 1 program, with addresses and annotations. The program, as written will emulate a Micro Term model ACT-4 video terminal. However, with the table of escape and control character equates at the beginning, it should be quite simple to modify the listing for any other codes. It is even possible to use any control and/or escape character for the same function. The program occupies about 1100 bytes, and thus there is plenty of room for any embellishments desired. The listing is self-explanatory; Zilog mnemonics are used. xx = version no.

VIDEOxx.Z80 ---

Same as above, but without address listing for use with Z80 assemblers. Provided only on 8 inch CP/M disk.

VIDEOxx.DTA ---

The object code for above, with origin at 00H. Load with DDT, and offset to a clear portion of ram for your prom-burner device.

CHARGEN.PRN ---

This is a HEX listing of each character block in ROM 2. Each 16 consecutive addresses defines one character from top to bottom, though only the first 10 bytes in each block is used, and the first is always zero. The overall matrix size is 9x7, though 5x7 is used for alpha-numeric.

CHARGEN.DTA ---

Same as above, but in BINARY format to load into system ram at 100H. Supplied on disk only.

CRTLOOP.Z80 ---

This is a demonstration program to exercise the VDB-A I/O ports, and to output video to the monitor device. The program tests both the system keyboard and the VDB-A keyboard port for data, and then outputs the data to the VDB-A, after first checking its status. If a host system keyboard driver program is to be used, just replace the IN (PORT) instructions with CALL (ADDR.) to those routines.

```

0000
0000
0000 ; CRTLOOP.Z80
0000
0000
0000
0000
0000 ; ROUTINE TO TEST CRT PORTS
0000 ; VERSION 1.1 12-30-82
0000 ;
0000 ; ORG=100H & 8080 FORMAT
0000 ;
0000 CRTS EQU 0F9H ;HOST SYSTEM KEYBOARD STATUS PORT
0000 CRTIN EQU 0FAH ;HOST SYSTEM KEYBOARD DATA PORT
0000 CRT0 EQU 0F0H ;VDB-A STATUS OUT/ DATA INPUT PORT
0000 CRTIN2 EQU 0F2H ;VDB-A KEYBOARD DATA PORT
0000 CRTS2 EQU 0F1H ;VDB-A KEYBOARD STATUS PORT
0000 ;
0100 ORG 100H
0100 ;
0100 DBF9 START: IN A,(CRTS) ;CHECK STATUS OF HOST KEYBOARD
0102 17 RLA ;ROTATE TO CARRY
0103 DA1101 JP C,CRT1 ;NO-CONTINUE
0106 DBF1 IN A,(CRTS2) ;CHECK VDB-A KEYBOARD STATUS
0108 17 RLA
0109 D20001 JP NC,START ;NO DATA - START OVER
010C DBF2 IN A,(CRTIN2) ;YES - GET DATA
010E C31301 JP CTLC
0111 DBFA CRT1: IN A,(CRTIN) ;YES-GET DATA
0113 FE03 CTLC: CP 3 ;CTL-C CHECK
0115 CA0000 JP Z,0 ;REBOOT TO CP/M
0118 4F LD C,A ;TEMP STORE
0119 DBF0 CRTOUT: IN A,(CRT0) ;CHECK STATUS
011B 17 RLA ;ROTATE TO CARRY
011C DA1901 JP C,CRTOUT ;NO-TRY AGAIN
011F 79 LD A,C ;GET DATA
0120 D3F0 OUT (CRT0),A ;SEND DATA
0122 3E00 LD A,0 ;FOR NEATNESS
0124 C30001 JP START ;LOOP
0000 END

```

```

0111 CRT1 00FA CRTIN 00F2 CRTIN2
00F0 CRT0 0119 CRTOUT 00F9 CRTS
00F1 CRTS2 0113 CTLC 0100 START

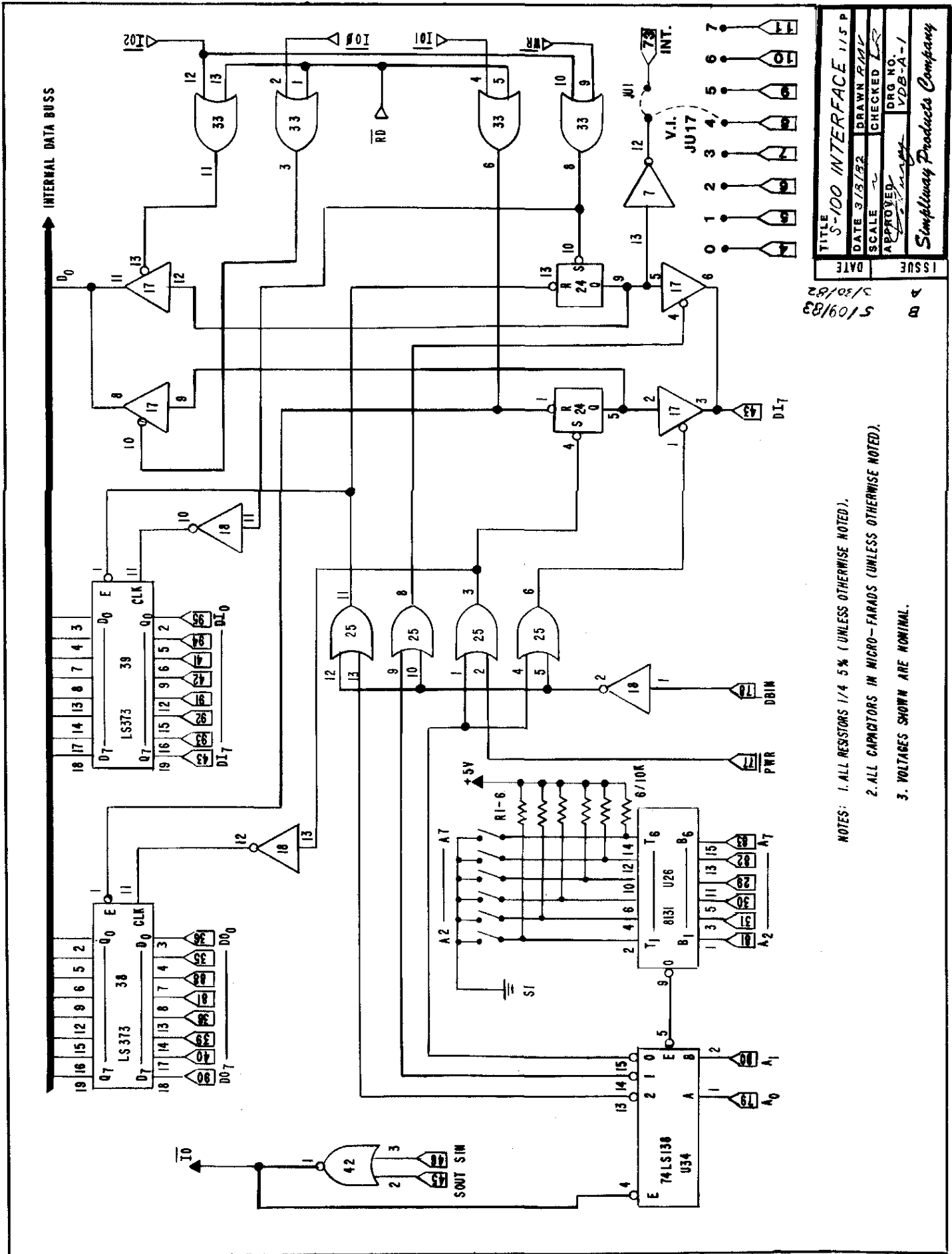
```

00 ERRORS

0340	00081828487C08080000000000000000	' 4 '
0350	007C4040780404780000000000000000	' 5 '
0360	00384440784444380000000000000000	' 6 '
0370	007C0408101010100000000000000000	' 7 '
0380	00384444384444380000000000000000	' 8 '
0390	003844443C0444380000000000000000	' 9 '
03A0	00000030300030300000000000000000	' : '
03B0	00000030300030302040000000000000	' ; '
03C0	00081020402010080000000000000000	' < '
03D0	0000007C007C00000000000000000000	' = '
03E0	00201008040810200000000000000000	' > '
03F0	00384404081000100000000000000000	' ? '
0400	003C448AAABC403E0000000000000000	' @ '
0410	00102844447C44444000000000000000	' A '
0420	00784444784444780000000000000000	' B '
0430	00384440404044380000000000000000	' C '
0440	00784444444444780000000000000000	' D '
0450	007C40407840407C0000000000000000	' E '
0460	007C4040784040400000000000000000	' F '
0470	00384440405C44380000000000000000	' G '
0480	004444447C4444440000000000000000	' H '
0490	007C10101010107C0000000000000000	' I '
04A0	003C080808084B300000000000000000	' J '
04B0	00444850605048440000000000000000	' K '
04C0	004040404040407C0000000000000000	' L '
04D0	00446C54544444400000000000000000	' M '
04E0	00444464544C44440000000000000000	' N '
04F0	00384444444444380000000000000000	' O '
0500	00784444784040400000000000000000	' P '
0510	00384444445448340000000000000000	' Q '
0520	00784444785048440000000000000000	' R '
0530	00384440380444380000000000000000	' S '
0540	007C1010101010100000000000000000	' T '
0550	00444444444444380000000000000000	' U '
0560	00444444444428100000000000000000	' V '
0570	0044444454546C440000000000000000	' W '
0580	00444428102844440000000000000000	' X '
0590	00444428101010100000000000000000	' Y '
05A0	007C04081020407C0000000000000000	' Z '
05B0	00382020202020380000000000000000	' ['
05C0	00804020100804020000000000000000	' \ '
05D0	00380808080808380000000000000000	'] '
05E0	00102844000000000000000000000000	' ^ '
05F0	00000000000000FE00000000000000000	' _ '
0600	00303010080000000000000000000000	' ` '
0610	00000038043C443C0000000000000000	' a '
0620	00404078444444780000000000000000	' b '
0630	00000038444040380000000000000000	' c '
0640	0004043C4444443C0000000000000000	' d '
0650	00000038447840380000000000000000	' e '
0660	00102820702020200000000000000000	' f '
0670	00000438444444380478000000000000	' g '
0680	00404070484848480000000000000000	' h '
0690	00100030101010380000000000000000	' i '
06A0	00080018080808082810000000000000	' j '
06B0	00404048506050480000000000000000	' k '

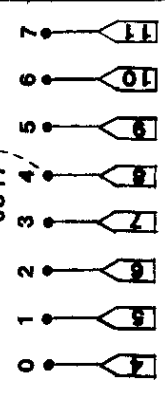
Troubleshooting Hints for the VDB-A Video Display Board

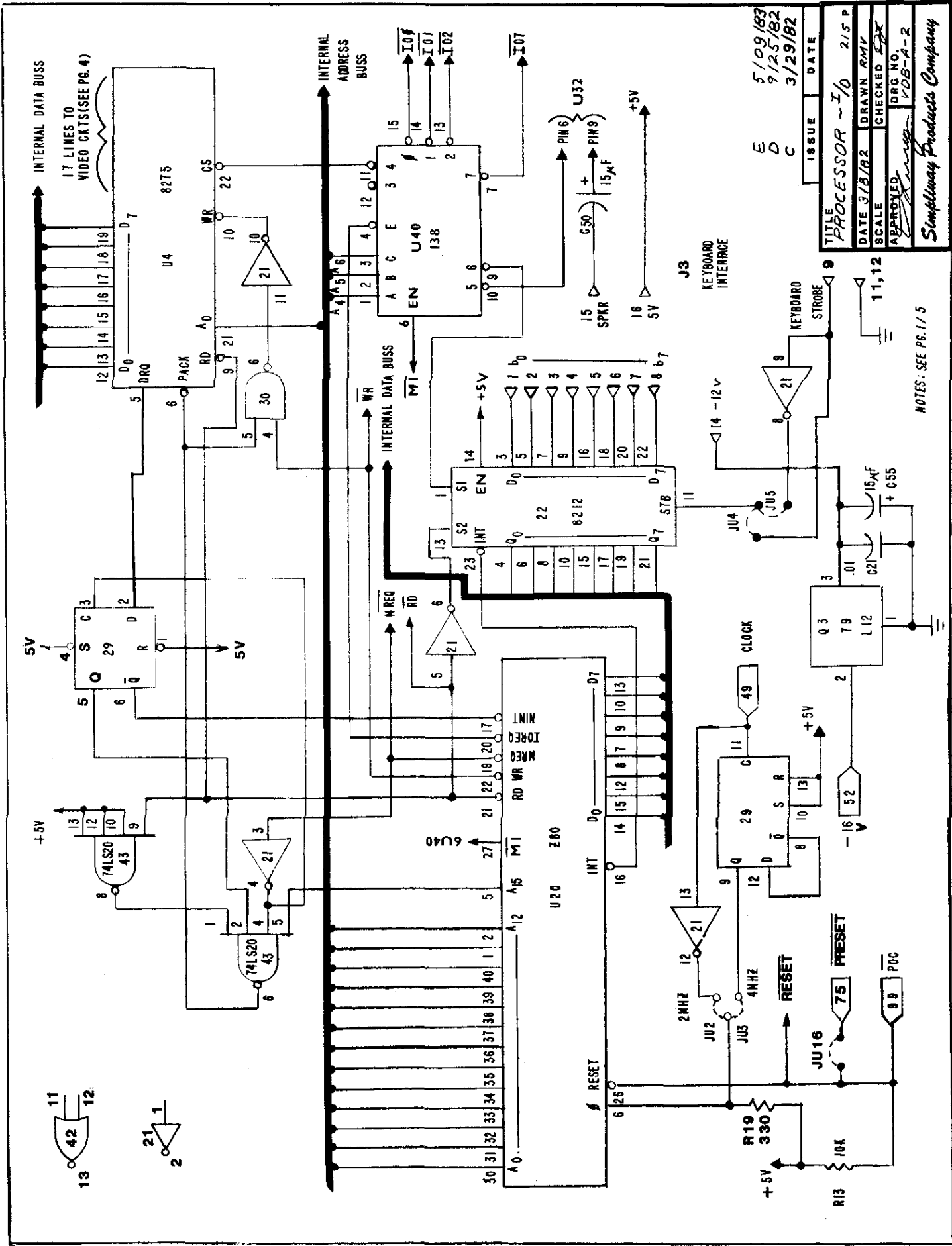
Problem	Probable Cause
1. No Sync on Screen	1a. Adjust Sync Pots b. No POC c. bad 8275, U4. d. check sync ckts e. Program not executing
2. No Character on Screen & Cursor does not move	2a. I/O address wrong b. Check S100 interface circuits
3. No Character on Screen but cursor moves ok	3a. 8275, U4, not sending DRQ b. Z80, U20, not accepting NMI c. NMI flip-flop not being set or reset
4. No keyboard response	4a. Strobe not getting to 8212, U22, or wrong polarity b. Z80, U20, not accepting INT c. Check operation of S100 interface circuits
5. No attributes, or only some missing	5a. check outputs of 8275, U4 b. check 74LS125, U17, and video summing circuits
6. Z80, U20, seems lost - random chars. on screen	6a. check RAM and ROM and Z80 b. address line foil shorts
7. Memory Map wrong address	7a. Wrong address selected b. screen parameters not matched c. check address latches
8. Memory Map not working	8a. enable flip-flop not set
9. Ready line not setting or releasing	9a. status flip-flop not working
10. Cursor lags behind character or every 8th char. repeats	10a. raise C48 to .001 uF. (VDB-A & -A1 revisions only)
11. Crystal won't start, or is erratic.	11a. replace U3, 74LS04 b. change U3 to a 7404.
12. Multiple cursors, spread out char's unstable display	12a. Monitor must be adjusted or modified to get 19 kHz horiz. sync frequency: R-C network in horiz osc changed
13. character line tears	13a. increase value of C54 to 47uF
14. scan line jitters on warm-up; char shifts (VDB-A & -A1 only)	14a. Change C14 to .0022uF poly styrene b. replace U23



- NOTES: 1. ALL RESISTORS 1/4 5% (UNLESS OTHERWISE NOTED).
 2. ALL CAPACITORS IN MICRO-FARADS (UNLESS OTHERWISE NOTED).
 3. VOLTAGES SHOWN ARE NOMINAL.

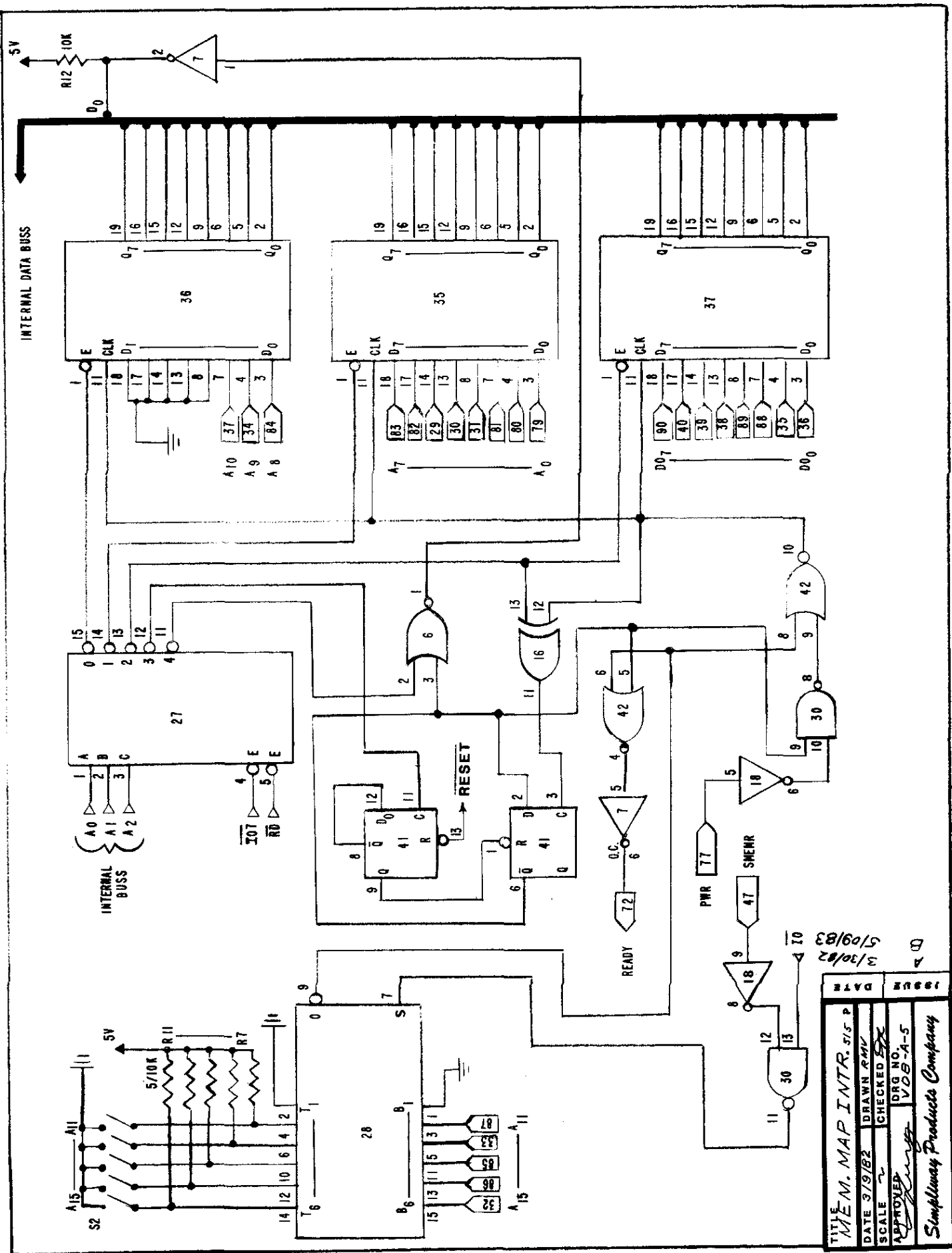
TITLE	S-100 INTERFACE 115 P
DATE	3/18/82
SCALE	DRAWN RRP
APPROVED	CHECKED IS
ISSUE	5/10/83
DATE	5/30/82
ISSUE	B
APPROVED	<i>[Signature]</i>
DRG NO.	VDB-A-1
Simpliway Products Company	





5/09/83	DATE
9/25/82	ISSUE
3/29/82	DATE
E	ISSUE
D	DATE
C	DATE
TITLE PROCESSOR ~ I/O 2.5 P.	
DATE 3/8/82	DRAWN RMP
SCALE	CHECKED <i>SPK</i>
APPROVED <i>[Signature]</i>	DRG NO. VDB-A-2
Simplway Products Company	

NOTES: SEE PG. 1 / 5



A
 3/30/82
 B
 5/09/83

ISSUE	DATE
1	3/30/82
2	5/09/83

TITLE MEM. MAP INTR. 515 P
 DATE 3/9/82 DRAWN RMP
 SCALE 1:1 CHECKED BX
 APPROVED *[Signature]* DRG NO. VDB-A-5
 Simplway Products Company

TO ORDER: Please check the items desired: May. 30, 1984

- VDB-A2 Video Board can be ordered in 3 ways:
- Bare board with standard 24 x 80 source code, includes heat sink and phono connector. \$ 49.50
 - Complete kit less crystal & eproms (Order eproms & crystal to match Rel. #, below) \$197.50
 - Assembled & soldered, but WITHOUT IC's/eproms you get your own & test. (state crystal Freq) \$182.50

- VDB-A2 Assembled and tested, with programmed eproms
- With standard 24 x 80 source code \$269.00
 - With VIDSTAR (Wordstar/dBase II) source code 279.00
 - With VIDSTAR 25th line non-scrolling, status "VIDSTAR" emulates the Televideo 920 terminal! 285.00

- ROM 1 Pre-programmed eproms for above source code
- Release 1.x : 24 lines x 80 characters, std. 18.50
 - Release 3.x : VIDSTAR for Wordstar / dBASE II 28.50
 - Release 4.x : VIDSTAR 25th line non-scrolling 32.50

- Character Generator eproms, 2716, 450 nS (ok at 4 MHz)
- ROM 2 Std. alpha-numeric, 5 x 7 matrix & 1-c 18.50
 - ROM 3 Graphics, Greek, a Potpourri (no source) 18.50

- Source and Data on 8" SSSD CP/M(tm) Disc (inc ROM 2)
- Release 1.x : 24 lines x 80 characters, std. 8.50
 - Release 3.x : VIDSTAR for Wordstar / dBASE II 22.75
 - Release 4.x : VIDSTAR with 25th line nonscroll 27.75

- Crystals, HC-18 size, wire leads, for Rel's 1.x & 3.x
- 13.628 MHz crystal (60 Hz. - USA) 18.9kHz 7.00
 - 11.357 MHz crystal (50 Hz. - foreign) 18.9kHz 9.00
- For Rel. 2.x (obsolete) and 4.x only :
- 11.340 MHz crystal (60 Hz. - USA) 15.7kHz 8.00
 - 9.4500 MHz crystal (50 Hz. - foreign) 15.7kHz 9.00

- Miscellaneous
- Serial Keyboard port adapter ** T.B.A.
 - LP-A LIGHT PEN for the VDB-A ** T.B.A.
 - Trim-pot set (2 - 20kohm, 1 - 5kohm) 4.50
 - 8275 CRT controller IC 27.75
 - Complete set of IC's & Q1, less eproms 73.00

Documentation	Complete	source only
<input type="checkbox"/> Release 1.x,	10.00	5.00
<input type="checkbox"/> Release 3.x,	16.00	11.00
<input type="checkbox"/> Release 4.x,	20.00	15.00
<input type="checkbox"/> No source list	5.00	-----
(refundable with VDB-A purchase) + 1.50 S&H -----		

Please add \$3.00 for shipping & handling 3.00

(Ill. residents please add 7% sales tax) -----

Prices subject to change without notice TOTAL -----

VISA / MASTERCARD NO. -----

Expiration date ----- Init. -----

Send C.O.D. Payment enclosed Amount \$ -----

Mail to: SIMPLIWAY PRODUCTS CO. or Phone:
P.O. Box 601 (312) 359 - 7337
Hoffman Estates, Il.
60195 ** COMING SOON !!



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Ship To: Name -----
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HOFFMAN ESTATES, IL 60195

HOW TO CONFIGURE 'WORDSTAR' & 'dBASE II' FOR THE SIMPLIWAY VDB-A VIDEO BOARD Releases 3.x & 4.x

Using the control codes that come standard with your Simpliway Video Board, configure your Wordstar in the following manner. With the INSTALL program, configure Wordstar to use the Televideo 912/920 terminal and the printer you are using. After you have installed the terminal and printer, enter the patch area by answering 'ND' to the prompt, and make the following changes:

ADDRESS	DATA
=====	=====
ERAEOL:	2
ERAEOL:+1	1B
ERAEOL:+2	54
LINDEL:	2
LINDEL:+1	1B
LINDEL:+2	52
LININS:	2
LININS:+1	1B
LININS:+2	45
DELCUS:	0
DELMIS:	0

Now save your Wordstar by typing 'O' and 'Y'.

Your Simpliway Video Board can now take advantage of all of the Televideo 912/920 terminal features offered by Wordstar.

Installing DBASE II

1. Install Televideo 920 terminal
2. Change clear screen command from 'ESC- *' to 'ESC- Z'.


```

0198 E3 CH1: EX (SP).HL ;WASTE TIME
0199 E3 EX (SP).HL ;LOOP TILL DONE
019A 10FC DJNZ ;DEC WAIT COUNT
019C 3D DEC A
019D 18F3 JR CHECK
019F C5 BC ;SAVE REGISTERS
01A0 D5 PUSH DE
01A1 E5 PUSH HL
01A2 F3 DI
01A3 DB41 IN A,(CRTO)
01A5 DB41 IN A,(CRTO)
01A7 E620 AND Z,CRTWT
01A9 28FA JR Z,CRTWT
01AB 2A0012 LD HL,(SCRTRL)
01AE E5 PUSH HL
01AF 210212 LD HL,SCRTRL+2
01B2 110012 LD DE,SCRTRL
01B5 012E00 LD BC,46
01B8 EDE0 LDIR
01BA E1 POP
01BB 22E12 LD HL,(SCRTRL+46),HL
01BE CBFC RES 7,H
01C0 3AD741 LD A,(MMSTUS)
01C3 FE00 CP 0
01C5 280B JR Z,DMAFIL
01C7 0650 LD B,B0
01C9 3620 LD HL,(HL),
01CB 23 INC HL
01CC 10FB DJNZ SPALF
01CE 0610 LD B,16
01D0 1802 JR BKLP
01D2 0660 DMAFIL: LD B,%6
01D4 36F1 LD HL,(HL),ENDDMA
01D6 23 INC HL
01D7 10FB DJNZ BKLP
01D9 FE EI
01DA E1 POP
01DB D1 POP
01DC C1 POP
01DD 0D DEC C
01DE C9 RET
01DF ;
01DF ; CALCULATES NEW LINE ADDRESS
01DF ;
01DF ; This routine calculates the refresh memory
01DF ; address of the first character in the line
01DF ; designated in register C
01DF ;
LNADDR: PUSH BC
01E0 D5 DE
01E1 0600 LD B,0
01E3 CB01 RLC C
01E5 210012 LD HL,SCRTRL
01E8 09 ADD HL,BC
01E9 5E LD E,(HL)
01EA 23 INC HL
01EB 56 D,(HL)
01EC EB DE,HL
01ED CBBC RES 7,H
01EF D1 POP
01F0 C1 POP
01F1 C9 RET
01F2 ; FILL ROUTINE
01F2 ;
01F2 ; This routine removes all of the end of line
01F2 ; code from in front of the cursor. This is done
01F2 ; so that new characters will be visible on that
01F2 ; line. This routine also counts the invisible
01F2 ; attributes and adjusts the pointer address.
01F2 ;
FILL: PUSH DE ;SAVE REGISTERS
01F3 E5 HL
01F4 0600 LD B,0
01F6 7E LD A,(HL)
01F7 E6C0 AND 0C0H ;GET CHARACTER
01F9 FE00 CP 0C0H ;STRIP 4 LSB
01FB 2002 JR NZ,NODMA ;IS IT A DMA CONTROL
01FD 3620 LD HL,(HL),
01FF 10 DEC E
0200 FA002 M,NOTILL
0203 FE80 CP 80H
0205 2002 JR NZ,NOTATT
0207 04 INC B
0208 1C INC E
0209 23 NOTATT: INC HL
020A 18EA LD HL,FLOOP
020C E1 POP HL
020D 58 LD E,B
020E 19 ADD HL,DE
020F D1 POP
0210 D9 RET
0211 ;
0211 ; INITIALIZE ALL CRT FIRMWARE
0211 ;
0211 ; This routine sets-up the CRT controller
0211 ; prepares the RAM area and initializes the
0211 ; cursor.
0211 ;
INITST: LD HL,TFPSCR+24*98 ;LOAD BEGINNING OF STATUS LINE
0214 0660 LD B,%6 ;LOAD LINE COUNT
0216 3620 LD HL,(HL), ;PUT SPACES
0218 23 INC HL ;ADVANCE POINTER
0219 10FB DJNZ STINLP
021B 36F0 LD HL,ELCODE ;LOAD EOL CODE
021D 216B11 LD HL,TFPSCR+(24*98)+79-(PARTBL-LOGON)
0220 117602 DE,LOGON
0223 1A LD A,(DE)
0224 FE00 CP 0 ;IF ZERO STOP
0226 2805 JR Z,INTORT
0228 77 LD HL,(HL),A ;PUT ON SCREEN
0229 23 INC HL ;ADVANCE POINTERS
022A 13 INC DE
022B 18F6 JR MSG
022D ;
022D ; INTORT: LD A,CRTEI ;ENABLE CRT INTERRUPT
022F 0341 OUT (CRTO),A ;(CRTO),A
0231 FD210012 LD IY,SCRTRL ;LOAD TOP OF TABLE
0235 ;

```

```

0235 01D0F6 CLS: LD BC, 98*24 ;LOAD COUNTER
0238 210008 LD HL, TOPSCR ;LOAD TOP A
023B 36F1 (HL), ENDDMA ;FILL MEMORY WITH END DMA
023D 23 HL ;
023E 03 INC ;COUNTER EQ ZERO?
023F 03 BIT 7, B ;
0241 20F8 JR NZ, INTLF ;LOAD COUNTER
0243 0618 LD B, 24 ;POINT AT END OF LINE
0245 216008 HL, TOPSCR+96 ;LOAD OFFSET PER LINE
0248 116200 DE, 98 ;DENOTES END OF LINE
024B 36F0 ATLOP: LD (HL), ELCODE ;ADD OFFSET FOR NEXT LINE
024D 19 HL, DE ;
024E 10F5 DJNZ ATLOP ;LOOP TILL 24 LINES DONE
0250 ;
0250 013800 LD BC, DLEND-15CRTBL ;INITIALIZE SCRTBL
0253 110012 LD DE, SCRTBL ;
0256 218E02 LD HL, 15CRTBL ;
0259 EDB0 LD LR ;
025B ;
025B 2A0012 LD HL, (SCRTBL) ;GET FIRST LINE ADDRESS
025E CBB0 RES 7, H ;RESET DMA BIT
0260 3E80 LD A, 80H ;CLEAR ATTRIBUTE BYTE
0262 320811 LD (ATLBUF), A ;
0265 0E00 LD C, 0 ;INITIALIZE REGISTERS
0267 51 LD D, C ;
0268 41 LD B, C ;
0269 59 LD E, C ;
026A CDE602 CALL CURSOR ;INITIALIZE CURSOR
026D ;
026D 3AD711 LD A, (MMSTATUS) ;IF MEM MAP ON FILL SPACES
0270 FE00 CP 0 ;
0272 4AF706 CALL NZ, MPMFILL ;YES - PUT SPACES
0275 09 RET ;
0276 ;
0276 ; CRT SCREEN PARAMETER TABLE
0277 564422D41322056657220342E30 ;SCREEN CONTROL PARAMETERS
0278 ;
0278 8020F32000 DEFB 80H, 20H, 0F3H, 20H, 00H ;LINE TABLE FOR SCREEN REFRESH
PARTBL: DEFB HCR ;
DEFB VVVR ;
DEFB ULL ;
DEFB MFCB ;
;
ISCTBL: DEFW TOPSCS ;
DEFW TOPSCB+98 ;
DEFW TOPSCS+98*2 ;
DEFW TOPSCB+98*3 ;
DEFW TOPSCB+98*4 ;
DEFW TOPSCB+98*5 ;
DEFW TOPSCB+98*6 ;
DEFW TOPSCB+98*7 ;
DEFW TOPSCB+98*8 ;
DEFW TOPSCB+98*9 ;
DEFW TOPSCB+98*10 ;
DEFW TOPSCB+98*11 ;
DEFW TOPSCB+98*12 ;
DEFW TOPSCB+98*13 ;
028A 4F DEFB 80H, 20H, 0F3H, 20H, 00H ;LINE TABLE FOR SCREEN REFRESH
028B 58 DEFB HCR ;
028C 79 DEFB VVVR ;
028D 09 DEFB ULL ;
028E DEFB MFCB ;
;
ISCTBL: DEFW TOPSCS ;
DEFW TOPSCB+98 ;
DEFW TOPSCS+98*2 ;
DEFW TOPSCB+98*3 ;
DEFW TOPSCB+98*4 ;
DEFW TOPSCB+98*5 ;
DEFW TOPSCB+98*6 ;
DEFW TOPSCB+98*7 ;
DEFW TOPSCB+98*8 ;
DEFW TOPSCB+98*9 ;
DEFW TOPSCB+98*10 ;
DEFW TOPSCB+98*11 ;
DEFW TOPSCB+98*12 ;
DEFW TOPSCB+98*13 ;
029A 4F DEFB 80H, 20H, 0F3H, 20H, 00H ;LINE TABLE FOR SCREEN REFRESH
029B 58 DEFB HCR ;
029C 79 DEFB VVVR ;
029D 09 DEFB ULL ;
029E DEFB MFCB ;
;
ISCTBL: DEFW TOPSCS ;
DEFW TOPSCB+98 ;
DEFW TOPSCS+98*2 ;
DEFW TOPSCB+98*3 ;
DEFW TOPSCB+98*4 ;
DEFW TOPSCB+98*5 ;
DEFW TOPSCB+98*6 ;
DEFW TOPSCB+98*7 ;
DEFW TOPSCB+98*8 ;
DEFW TOPSCB+98*9 ;
DEFW TOPSCB+98*10 ;
DEFW TOPSCB+98*11 ;
DEFW TOPSCB+98*12 ;
DEFW TOPSCB+98*13 ;
02AA 5C8D DEFW TOPSCB+98*14 ;
02AC 8EBD DEFW TOPSCB+98*15 ;
02AE 208E DEFW TOPSCB+98*16 ;
02B0 828E DEFW TOPSCB+98*17 ;
02B2 848E DEFW TOPSCB+98*18 ;
02B4 468F DEFW TOPSCB+98*19 ;
02B6 488F DEFW TOPSCB+98*20 ;
02B8 0A90 DEFW TOPSCB+98*21 ;
02BA 6C90 DEFW TOPSCB+98*22 ;
02BC CE90 DEFW TOPSCB+98*23 ;
02BE 3091 DEFW TOPSCB+98*24 ;
02C0 0000 DEFW 0000 ;
WDMOVE: LD (DUMMY), HL ;SWAP LINES IN TABLE
; TO PREVENT FLASHING
DLEND: RET ;
RMDMOV EDU WDMOVE-15CRTBL+SCRTBL ;ADDRESS OF WORD LOAD
; MOVE CURSOR ROUTINE
; This routine moves the cursor on the screen
; based on the data in registers C & E.
CURSOR: LD A, CURPOS ;SEND CONTROL CHAR
OUT (CRTC), A ;
LD A, E ;SEND COLUMN
OUT (CRTD), A ;
LD A, C ;SEND LINE
OUT (CRTD), A ;
LD A, (HL) ;SEE IF DMA
AND 0F0H ;STRIP LSB'S
CP 0F0H ;
RET NZ ;NO RETURN
LD (HL), ' ' ;PUT SPACE SO CURSOR WILL APPEAR
;
; KEYBOARD BUFFER TO S100 SERVICE ROUTINE
; This routine checks the S100 keyboard port
; status and return if busy or loads the port
; with the next character in the keyboard
; buffer.
KEYOUT: IN A, (KYS100) ;CHECK STATUS
RET ;NOT READY RETURN
PUSH C ;SAVE HL
LD HL, (KYDTA) ;GET OUTPUT BUFFER ADDR
DEC (IX+0) ;DEC COUNTER
LD A, L ;CHECK ADDR AT BOTTOM
BOTKEY CP ;NO THEN SKIP
JR NZ, NOBOT1 ;POINT TO TOP
LD HL, TOPKEY ;GET CHARACTER
LD A, (HL) ;(KYS100), A
INC HL ;INC POINTER
LD (KYDTA), HL ;SAVE POINTER
POP C ;RESTORE HL
NOBOT1: LD A, (KYS100), A
INC HL
LD (KYDTA), HL
POP C
;
; ATTRIBUTE CONTROL ROUTINES
;
02C5 09 RET ;
02C6 ;
02C6 ;
02C6 ;
02C6 ;
02C6 ;
02C6 ;
02C6 3E80 LD A, CURPOS ;SEND CONTROL CHAR
02C8 D341 OUT (CRTC), A ;
02CA 7E LD A, E ;SEND COLUMN
02CB D340 OUT (CRTD), A ;
02CD 79 LD A, C ;SEND LINE
02CE D340 OUT (CRTD), A ;
02D0 7E LD A, (HL) ;SEE IF DMA
02D1 E6F0 AND 0F0H ;STRIP LSB'S
02D3 FE00 CP 0F0H ;
02D5 C0 RET NZ ;NO RETURN
02D6 3620 LD (HL), ' ' ;PUT SPACE SO CURSOR WILL APPEAR
02D8 09 RET ;
02D9 ;
02D9 ; KEYBOARD BUFFER TO S100 SERVICE ROUTINE
02D9 ; This routine checks the S100 keyboard port
02D9 ; status and return if busy or loads the port
02D9 ; with the next character in the keyboard
02D9 ; buffer.
02D9 KEYOUT: IN A, (KYS100) ;CHECK STATUS
02DB 1F RET ;NOT READY RETURN
02DB 08 PUSH C ;SAVE HL
02DD E5 LD HL, (KYDTA) ;GET OUTPUT BUFFER ADDR
02DE 2AD511 DEC (IX+0) ;DEC COUNTER
02E1 DC3500 LD A, L ;CHECK ADDR AT BOTTOM
02E4 7D BOTKEY CP ;NO THEN SKIP
02E5 FED0 JR NZ, NOBOT1 ;POINT TO TOP
02E7 2003 LD HL, TOPKEY ;GET CHARACTER
02E9 21A011 LD A, (HL) ;(KYS100), A
02EC 7E INC HL ;INC POINTER
02ED D320 LD (KYDTA), HL ;SAVE POINTER
02EF 23 POP C ;RESTORE HL
02F0 22D511 LD A, (KYS100), A
02F3 E1 INC HL
02F4 09 LD (KYDTA), HL
02F5 RET ;
02F5 ;
02F5 ; ATTRIBUTE CONTROL ROUTINES
02F5 ;

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D3
20

07BB 00	DEFB	EGRF	03FF	DORTWT	03D3	DELLN	0421	DFIL
07BC 00	DEFB	EHTOG	02C6	DLEND	053B	DMA1	01D2	DMAFIL
07BD 00	DEFB	EOLDFN	0545	DMAOVR	0030	DMA1	0407	DMAOVR
07BE 00	DEFB	00	0418	DSELP	06C9	DTAOUT	0000	DUMMY
07BF	:	ATTRIBUTE	0058	EALICH	0000	ERELL	005E	EBLINK
07BF	:	JUMPF	0000	ECURDN	0000	ECURLT	0000	ECURRT
07BF	:	TABLE	0054	EEDL	0052	EDELLN	05D4	EDSON
07BF	:		0029	EHLITE	0059	EEDS	0000	EGRF
07BF	:		0000	EHTOG	005A	EHOME	0000	EHOMEUP
07C1 7804	DEFW	OLDNFN	0040	ELPEN	0045	EINLN	004F	EMEMO
07C3 9906	DEFW	GRAF	0071	ENBLNK	00F1	ENDDMA	002B	ENHLIT
07C5 2E04	DEFW	INLN	03B5	ENL	006B	ENRVID	0354	EOL
07C7 D203	DEFW	DELLN	0365	EOL1	037E	EOLATT	0000	EOLDPN
07C9 A804	DEFW	ALICH	039F	EGLEND	0395	EOLLP	039B	EOLVDR
07CB B406	DEFW	SOLWT	03B0	EOLSP	03AA	EOS	03BB	EGSLP
07CD A406	DEFW	RDCUR	003F	ERDCUR	006A	EREVID	001B	ESC
07CF 7407	DEFW	MEMO	0155	ESCAPE	0053	ESLWT	07A3	ESCTBL
07D1 0C07	DEFW	MEM	003D	ESTCUR	0138	EDMAT	0670	FDONE
07D3 8106	DEFW	LPEN	01F2	FILL	0672	FINDAT	01F6	FLOOP
07D5 A004	DEFW	NBLNK	0699	GRAF	004F	HCR	0468	HLITE
07D7 9804	DEFW	BLINK	02F5	HOME	045D	HOMUP	047B	HTOG
07D9 9004	DEFW	NRVID	044D	ICRTWT	042E	INLN	022D	INTCRT
07DB B804	DEFW	REVID	023B	INTLP	0211	INTST	028E	ISCTBL
07DD 7004	DEFW	NHLIT	0060	KEYBD	02D9	KEYOUT	11D3	KYINA
07E1 6404	DEFW	BELL	11D5	KYDTA	0020	KYS100	000A	LF
07E3 5D04	DEFW	HOMEUP	0177	LIFD	0060	LITP	01DF	LNADD
07E5 A403	DEFW	EOS	0400	LNFIL	0276	LOGON	0681	LPEN
07E7 6403	DEFW	EGL	0682	LFLP	070C	MEM	06DE	MEMINT
07E9 5C03	DEFW	CURLT	0776	MEMO	0519	MERGE	0009	MFCH
07EB 5403	DEFW	CURRT	0050	MMCOL	0752	MMCONT	0072	MMD
07ED 4903	DEFW	CURDN	0749	PMDIV	0073	MMEN	0770	MMEND
07EF 4103	DEFW	CURUF	0772	PMEND1	06F7	MMFILL	0070	MMH
07F1 F902	DEFW	STCUR	0071	PML	001B	MMLINE	0750	MMPOS
07F3 F502	DEFW	HOME	0074	PMS	0710	MMSTAT	11D7	MMSTUS
0000	THEEND:	END	0726	MOVIDE	00CF	MORINT	0624	MOVDRN
			0604	MOVEND	0612	MOVST	05EC	MOVSDR
05A9 ADMOVE	0591	ADJSCR	0223	PSC	060A	MVCHR	04A0	NBLNK
05B5 ATDOME	0516	ATDOME	0470	NHLIT	032F	N025	05B9	NOADJ3
11D8 ATTRUF	04B6	ATTFCH	0532	NOAT1	0045	NOROT	02EC	NOBOT1
11D9 ATFLB	05DD	ATTONE	0538	N02HG	01FF	NDDMA	0657	NOFDAT
0557 ATINMT	07BF	ATTEL	020C	NOFILL	0151	NOMAT	00B9	NOMORE
055A ATISP	0454	BELL	0455	NOMOVE	06C3	NO19	0209	NOTATT
00E4 BBS1AT	00D0	ROTKEY	05A1	NOTSAM	019F	NOWAIT	0490	NRVID
01D4 BLKLF	0007	CBELL	0000	NUL	065C	NXTATT	05F2	NXTMOV
0000 CALICH	0008	CDURLT	0020	OFFSET	06B2	OLDPN	05FB	OVAMOV
000A CCLURDN	0000	CDELLN	05B4	QVRSF	03E3	QVRSF	028A	PARTBL
000B CCLURUF	0000	CBELL	0111	FLCHAR	0331	FLCUR	04BF	PRATT
0000 CEGS	0016	CGRAF	0476	PRVAT1	0654	PRVATT	06A4	RDCUR
0198 CHI	0000	CHLITE	0484	RESETA	0484	RESETH	048B	REVID
001E CHOMUP	000E	CHT08	12C4	R2MOV	0000	S100ST	11DE	SAVECOL
031E CKCUR	0000	CLPEN	11DD	SAVLN	06B4	SCLWT	01BF	SCRLL
0000 CHEM	0000	CHEM	1200	SCRIBL	01C9	SPALP	06FC	SPCLP
0000 CNHLIT	0000	CNRVID	0050	SPEAK	058E	SPOVR	13A0	STACK
00C9 CONT1	000D	CR	00EC	STATUS	02F9	STCUR	0216	STINLP
0000 CREVID	0169	CRUF	00F3	STPDMA	0023	STRSCR	11DA	TEMP
0040 CRTD	00A0	CRTE1	11DB	TEMP2	1250	TEMLN	07F5	THEEND
0000 CSCLWT	0000	CSTCUR	062B	TFSCN	11A0	TOPKEY	8B00	TOPSC8
0135 CTRAF	0349	CURDN	0600	TOPSCR	0679	ULL	0010	VDS100
030D CURNAT	00B0	CURPOS	00FA	V1DED	005B	VVTR	02C2	WDMOVE
02C6 CURSOR	0341	CURUF	0164	WRAP	11D1	WTCTR		